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Resonant-Free PDN Design®

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Abstract—**The design of power distribution networks (PDNs) on printed circuit board (PCB) structures, or even on interconnect structures inside IC packages, typically results, with or without decoupling capacitors added, in a network full of impedance resonances. These resonances functionally hamper fast digital and RF**

designs from several MHz up to the GHz-range onwards and are the root cause for many EMC issues. These resonances are caused both by the physical size and geometry of the PCB and the decoupling as well as the loading components added to that PCB.

Utilizing the characteristic impedance of the adjacent supply and ground layers correctly, results in a resonant free supply PDN with an impedance which can be made very low over an extremely broad frequency range. This, in combination with 'Kelvin contact' decoupled ICs, assures that the low impedance of the PDN can be maintained and multiple decoupling capacitors are no longer needed near to the IC pins. This offers great advantages for PCB space allocation and opens opportunities to more efficient routing.

This extended concept has been verified by simulations. Additional measurements were taken to validate the concept.

Keywords: power distribution network (PDN), printed circuit board (PCB), power integrity (PI), signal integrity (SI) electromagnetic compatibility (EMC), resonant-free

I. INTRODUCTION

Numerous books [1-3], transactions [4], patents [5-11] and papers [12-25] about PCB design and decoupling strategies have been written and many approaches and design tools have been presented which quite often have resulted in a farm of decoupling capacitors to be put adjacent or underneath the IC to be supplied and decoupled, see the example in figure 1.

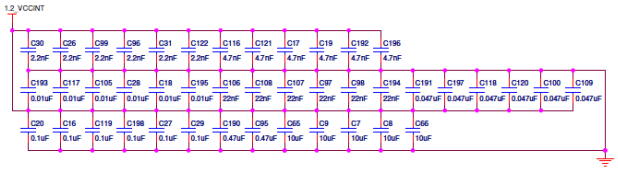

Figure 1 - Farm of decoupling capacitances

It is also known that multi-layer PCB structures can best be used with multiple ground and supply planes in parallel at the closest possible spacing, further improved by filling the dielectric in-between planes by high-dielectric but RF-lossy material [10-11]. These measures have in common that the PDN impedance can be brought down into the mΩ region up to 1 GHz and above to allow supply current changes in nanoseconds with only millivolts of supply ripple. Typically, charge takes time to travel over distance and decoupling capacitors need to be placed close to the IC. Alternatively, application of embedded on-chip or in-package decoupling capacitance is no longer uncommon [2, 3] and shall be utilized.

As on- and off-board voltage regulators (VRMs, LDOs) have limited bandwidth, the instantaneous supply current changes have to come from local charge buffering/decoupling capacitors for which the following well-known equations are used:

$$Q = C \cdot U, dQ = C \cdot dU$$

$$Q = i \cdot t \rightarrow dQ = i \cdot dt \vee t \cdot di$$

$$i_c = C \cdot \frac{dU}{dt}$$

$$U_L = L \cdot \frac{di}{dt}$$

To suppress a supply dip to less than 60 mV, which is 5% of the nominal supply voltage (typical for nanometer CMOS), a 1 ampere supply current step in 1 ns requires instantaneous charge from a local decoupling capacitor until the overall supply system is able to recharge, which typically takes 1 µs. Local charge buffering with a capacitance larger than 16,6 µF is needed to achieve this.

For a similar voltage dip over the effective package inductance towards the inside chip, the total inductance of the lead frame plus bond wires needs to be less than 60 pH (≈ 60 µm in length). When a physical path length of 2 mm for both ground and supply is taken, it would require 66 non-mutually coupled connections in parallel.

To assure a similar voltage dip in the supply in case of 1 ampere current change, the PDN on the PCB needs to be 60 mΩ at maximum. The total top-metal conductivity of a CMOS chip is about 20 mΩ-square. Only full utilization will result in an on-chip voltage bounce that is lower than the off-chip one.

An issue to be solved is that the 5% voltage dip margin applicable to those nanometer-scale ICs as a whole is spent more than 3 times, even while excluding resonances. Thus,

each of the voltage bounce effects are allowed to only a fraction of the maximum tolerable voltage dip.

Last but not least, the PCB supply and ground layers behave as a transmission line with 'praised' low characteristic impedance but typically with too little charge storage in-between these plates.

Chapter II discusses PCB transmission line effects and how these lines need to be terminated to benefit from their low impedances. The various implementations for termination networks will be discussed in chapter III. The integral resonant free PDN will be explained in chapter IV and the combination with 'Kelvin' contacts is given in chapter V. Measurement findings are addressed in chapter VI and in chapter VII the final conclusions are given.

II. TRANSMISSION LINES AND CHARGE BUFFERING

When transmission lines are left open, at the edge of the board in case of PCBs, the wave front propagating to the edge will be fully reflected and return at the excitation port after $2\tau_{pd}$. For any rectangular board, there will be unequal distances to the 4 board edges thus multiple reflected waves result. This effect can be explained by using a simple transmission-line model e.g. that of a coaxial line which is non-characteristically excited at one end but left open at the other side, see figure 2.

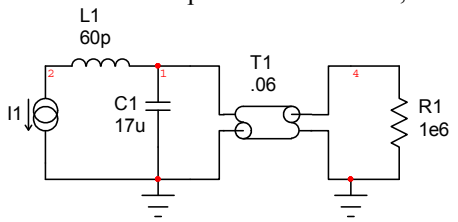

Figure 2 - Simple decoupling circuit with an open PCB transmission line

In this example, a step of 1 ampere is used and for the transmission line we assume τ_{pd} = 1 ns (approximately 0,14 m) and Z_0 = 60 mΩ. At the near-end (= IC-side including the current source) the initial supply voltage, 1,2 volt, is only taken into account as an initial voltage, no recharging is assumed.

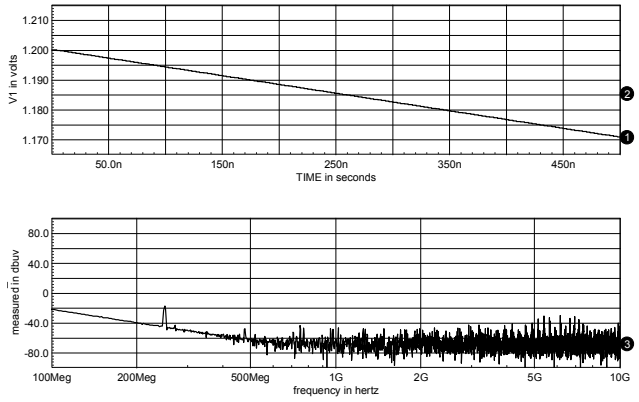

Figure 3 - V1 = near-end voltage (time domain), lower part is its FFT

This initial voltage is rippling down smoothly due to an ideal decoupling capacitance in parallel, see figure 3. At the far-end (= board edge), see figure 4, reflections/steep resonances occur which increases the open voltage by orders of magnitude compared to the excited ripple voltage at the near-end.

As can be seen from figures 3 and 4, the voltage at the far-end appears nearly 60 dB higher than at the near-end as resonances occur at 250 MHz and its odd harmonics (this is in an ideal lossless case). However, with the same transmission line terminated by its characteristic impedance, the far-end 'over' voltage diminishes to the result given in figure 5, an improvement of 20 dB compared to the near-end excitation and nearly 80 dB to the non-terminated far-end condition.

The open-ended situation as described does occur in all 4 directions of a rectangular PCB, most likely with 4 different propagation delays towards each board edge. When the transmission line is terminated correctly over the full width of the PCB edges, traveling wave conditions are met for all 4 directions. Furthermore, the excitation port now sees 4 identical terminated transmission lines in parallel, in each direction of propagation, which effectively divides the port impedance by a factor 4.

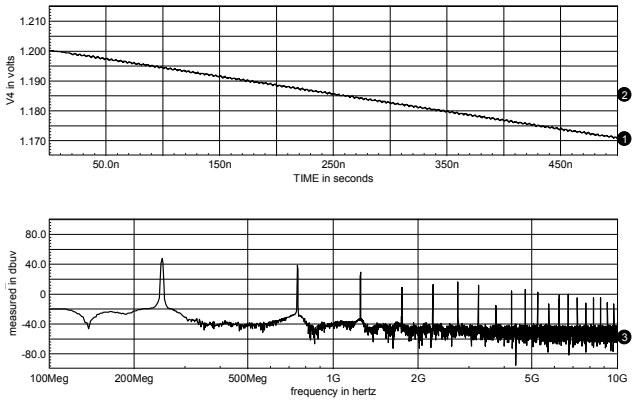

Figure 4 – V4 = far-end voltage (time domain), lower part is its FFT

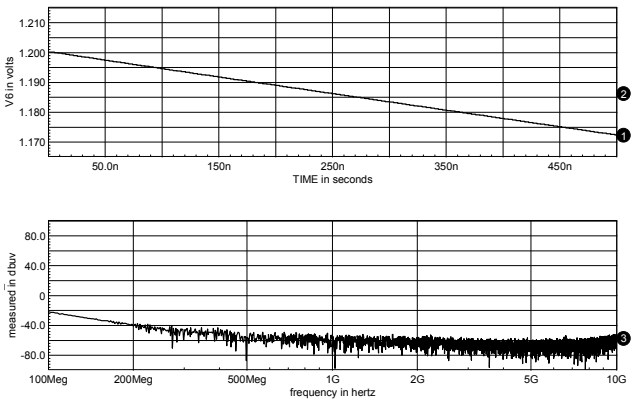

Figure 5 - V4 = far-end voltage (time domain) when terminated, lower part is its FFT

III. TERMINATION NETWORK

The concept as just described is easy to apply. The characteristic impedance of the transmission line formed between the supply and ground plane can be easily calculated

and will vary with the edge width, the dielectric insulating material thickness and its dielectric constant, real or complex (= with RF losses). Values between 2,7 Ω (1,6 mm FR-4) down to 0,17 Ω (100 µm FR-4) are found, which need to be divided by 4 at the excitation port. When high-dielectric insulating layers are used this impedance can be further reduced to several mΩ.

Each PCB edge needs to be terminated by a termination impedance equal to the characteristic transmission line impedance (unless the RF loss towards the edges are larger than 20 dB). These termination impedances have to be distributed over the full width of the PCB edges. As current density distributions at these board edges are unknown, a number of *N* equally-spaced RC-elements shall be used in parallel, either chosen as single 'hybrid' components or built from two lumped components in series. Best-case, resistive and capacitive silk materials can be applied around the full circumference of the PCB to establish the termination impedances needed. Do consider that characteristic impedances are not linearly proportional to the board width, so the combination of resistance and capacitance does differ per edge, this to satisfy the optimal termination conditions.

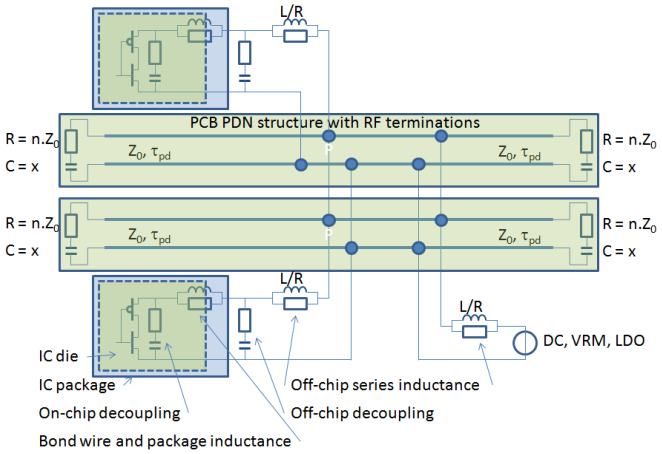

Figure 6 - Complete resonant-free PDN application structure using multiple supply ground pairs in parallel

Termination impedances can be built from lumped resistors and capacitors in series but a better way is to critically select these capacitors, as most ceramic multilayer capacitors have a non-negligible equivalent series resistance (ESR) which can be used to achieve the required termination resistance. ESR values can be found in the range from several mΩ to a few Ω. When 60 mΩ needs to be achieved, capacitors with an ESR = $N \cdot$ 60 mΩ shall be chosen, assuming *N* capacitors in parallel. The value of *N* is determined by the maximum frequency to which the concept has to apply. As a practical guidance, 10 capacitors per minimum wavelength (= $c_0/(\sqrt{\varepsilon_r} \cdot$maximum frequency)) will do. The equivalent series inductance (ESL) is less critical as it is determined by the physical length of the capacitor itself. This 'extra' component path length can be neglected compared to the path length in-between the termination impedances at the edges of the PCB in parallel.

The total amount of PDN decoupling capacitance, buffered charge: $N \cdot$ x, see figure 6, is determined by the circuits which will be placed on the PCB, as no direct decoupling capacitance is needed (nor allowed) adjacent to the IC as the PDN itself represents a near-to-infinite broadband low impedance. Local decoupling, as given in figure 6 is still allowed when conditions are met to sustain the resonant free PDN approach. This will be explained in the next chapters.

IV. Resonant-free PDN application structure

As can be seen from figure 6, being a 2-dimensional representation of the resonant-free PDN concept, each set of supply/ground layers is terminated at its boards edges. Multiple supply/ground layer pairs have to be connected in parallel at those nodes where low impedance PDN contacts are needed e.g. to connect devices or components or where signals have to cross these layers, this to serve ground return path continuity. Due to proximity effects (skin-effect), the opposite RF decoupling current distributions within these supply/ground layer pairs towards their termination impedances remain on the inside of these layer structures. Functional signals can therefore be referred to either supply/ground layer pairs as the decoupling currents are well-confined and low impedance coupled. Serious crosstalk between power and signals is therefore unlikely to occur.

The fact that the speed of charge transfer is limited to a fraction of the speed of light no longer plays a role in this application as the properly selected capacitors used take the short term effects into account: an infinitely long terminated transmission line is capable to deliver constant current. The amount of (decoupling) charge needed will be equal to the quest for on- or off-board voltage regulators to respond.

The R+L or R//L impedance of the lead frame plus bond wire towards a device has to be calculated. The combination of the inductance with the on-chip capacitance must be critically damped. Here it is assumed that the off-chip PDN impedance is determined to be 60 mΩ resistive. The total impedance of a device being connected to the PDN must be much higher to sustain the resonant- free PDN impedance.

On the other hand, the minimum slew rate occurring at the chip/package's resonance frequency will define the minimum off-chip current rise time, which is set to 1 ns and which needs to be critically to over-critically damped. The $R_{PDN}C_{on\text{-}chip}$-delay constant needs to be less or equal than 1 ns, e.g. an on-chip capacitance of 17 nF in combination with the 60 mΩ PDN impedance. The remaining LC-circuits still need to be critically damped: 60 pH package inductance results in a critically damped resonance at 158 MHz.

The equivalent output impedance of the DC source shall be high (at the frequencies above 10 MHz) compared to the total PDN impedance. This can be achieved by adding an RF-lossy

ferrite bead in series with the DC-source's output and the terminated PDN structure. Doing so makes the position of supply contacts to the PDN structure non-critical.

Having multiple capacitors in parallel, figure 1, without causing resonances is typically hard to realize in practice. In particular when a farm of capacitors is needed, capacitors with different values ranging from 100 µF to 100 pF can cause steep resonances at specific frequencies all over the frequency range. If four ceramic capacitors are placed 1 mm apart in parallel to a voltage regulator module, the dotted impedance curve in figure 7 results. At some frequencies the total impedance is less than the damped curve (solid line), which sounds good, but at other places it is higher, which is cumbersome when clocks or rare bit pattern harmonics coincide with these resonances. Such an application will often not work or be hampered occasionally.

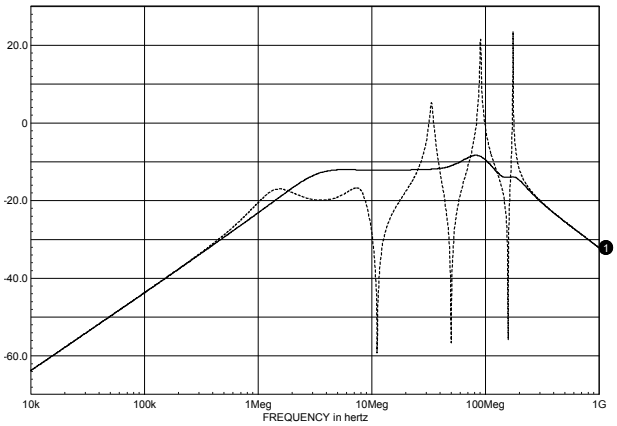

Figure 7 - Log impedance of parallel ceramic capacitors as function of frequency with (solid)/without (dotted) ESR [dBΩ]

V. KELVIN CONTACTS

By using 'Kelvin' contacts [26] for decoupling, the supply impedance requirements can be fully split into a high-impedance requirement for the average DC supply current path and a low-impedance requirement for the RF decoupling path through which the off-chip decoupling currents flow. The off-chip current ratio between the average DC supply current and the peak current may be as high as 25 to satisfy a CMOS electro-migration rule.

With 'Kelvin' contacts, the off-chip capacitor needs to be isolated from the ground layer of the PCB. The external capacitor needs to be placed in parallel to the on-chip circuit to be decoupled with low inductive bonding. To minimize the effective package series inductance, pairs of adjacent pins or balls shall be allocated which are also inside the package routed as adjacent traces or planes.

The effectiveness of the 'Kelvin' contact solution is also determined by the orientation of the IC's internal disturbance source. In the example of figure 8, a single disturbance source is taken in-line with the 'Kelvin' contact positions, which is best-case. If the internal disturbance source is orthogonal, the disturbance source becomes balanced in a 'Wheatstone bridge' topology formed by the on-chip DC supply ring. The net result for the ground bounce reduction will then be maximal. On-chip power routing and pin assignments have a crucial impact on the external noise that it should be supported by EDA tools, but most of these tools can't do it.

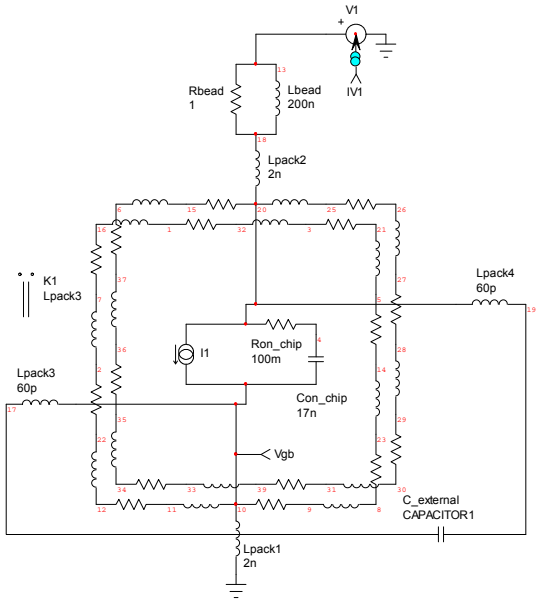

Figure 8 - Kelvin contact application

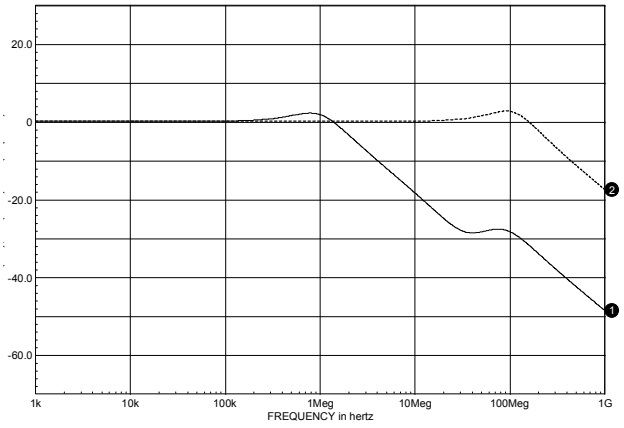

Figure 9 - Off-chip supply current reduction due to 'Kelvin' contacts

In figure 9, the difference in off-chip current is given between a decoupling design without 'Kelvin' contacts (dotted) and one using 'Kelvin' contacts (solid). A typical improvement of 30 dB is achieved at the higher frequencies.

The advantages of using 'Kelvin' contact decoupling are threefold:

- the off-chip disturbance currents will be reduced which will proportionally reduce the ground-bounce voltage
- an RF-lossy ferrite bead may be added in series with the IC's DC supply towards the PDN without affecting the low resonant-free PDN impedance as the flow of decoupling currents are confined

- the noise generated onto the PDN will be decimated as yet another order of filtering is achieved due to the additional series impedance of the ferrite bead.

When an RF series impedance of a few ohms is achieved by the ferrite bead at higher frequencies, the attenuation towards the PDN, assumed to be 60 mΩ, will be considerable.

Power integrity is met over the full frequency range of interest as soon as the local resonances are critically to over-critically damped, signal integrity is improved as the ground-bounce compared to conventional decoupling is decimated and EMC is, at the critical frequencies, improved by several orders of magnitude.

VI. MEASUREMENT RESULTS

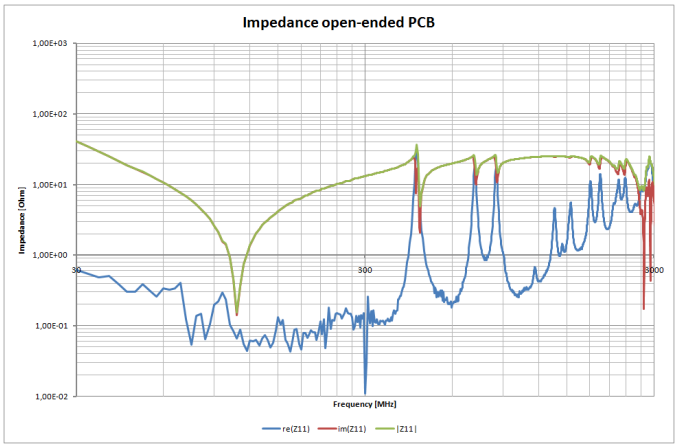

Figure 10 - Port impedance when PCB edge is left open-ended

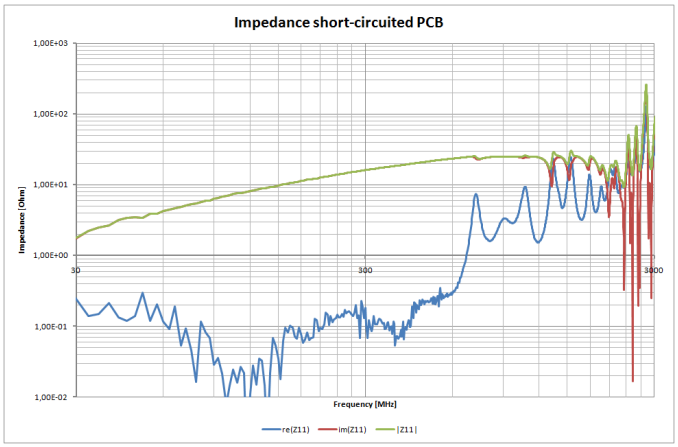

Figure 11 - Port impedance when using standard (low-ESR, low-ESL) ceramic decoupling capacitors at the edges

The resonant free PDN structure concept has been tested by using 3 Eurocard PCBs with an excitation port at an off-center location, figures 10-12, but the FR-4 board thickness 1,6 mm (equals 1,6 nH) has not been compensated for. The low-frequency impedance is 0,625 Ω (= 2,5 Ω/4) as can be calculated for the Eurocard PCB, FR-4 1,6 mm thick, see figure 12. Important to note is the achieved continuous absorptive impedance: re(Z_{11}) which damps most of the resonances present in figures 10, 11. In this example, only 26 terminations where used along the 0,52 m circumference of the Eurocard PCB.

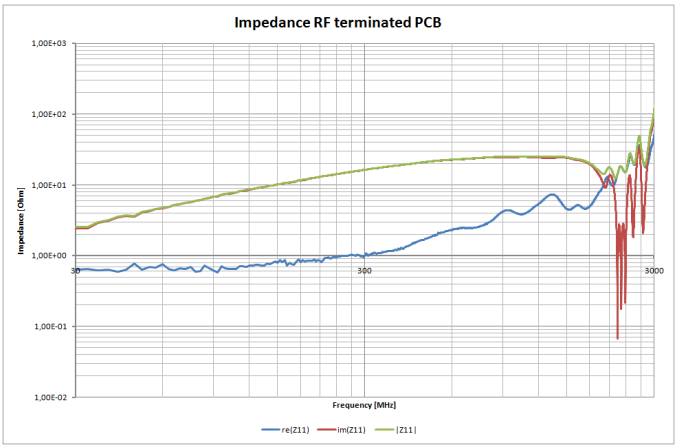

Figure 12 - Port impedance of an RF terminated Eurocard PCB using decoupling elements as described

VII. CONCLUSIONS

Resonant free PDN designs have been suggested and tried for several decades but they are rarely used in practice. No application constraints have been found.

PDN structures with less than 10 mΩ impedance over a GHz bandwidth can be achieved. By terminating supply and ground layers correctly, PDN resonances can be avoided and low impedance is achieved. The equivalent PDN impedance is determined by the layer topology, material and the number of ground/supply layers used in parallel.

The PDN decoupling capacitance shall provide sufficient charge buffering to bridge the time necessary until the VRM/LDO is able to correct for current changes on the PCB.

The PDN termination network can be achieved by using discrete components, properly selected capacitors or by using distributive silk processes.

All devices and connections made to the resonant-free PDN shall represent equivalent impedances higher than the PDN impedance itself.

Local IC decoupling, when necessary, shall be critically or over-critically damped, preferably in combination with 'Kelvin' contacts. Another order of crosstalk reduction can be achieved when ICs are provided with multiple supply and ground pads/pins for the various supply domains.

By combining both, resonant-free PDN design and 'Kelvin' contact IC decoupling, power integrity, signal integrity as well as EMC can be improved by an order of magnitude or more while effectively reducing PCB area and simplifying routing.

VIII. ACKNOWLEDGEMENT

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