Over the years, many papers and articles have been written about optimizing off-chip IC decoupling. Many IC vendor application recommendations feature a cluster of decoupling capacitors adjacent to the IC, in close proximity to one another—viz. an electrolytic capacitor along with a small and a large value ceramic capacitor at the various supply nodes. The basic conviction underlying this approach is that the decoupling impedance must be low over as broad a frequency range as possible.

In functional PCB design and IC applications, this approach holds true. However, when dealing with electromagnetic compatibility, an opposite track must be taken. In nearly all digital, as well as analog and RF designs, intentional on-chip decoupling capacitance is included—regardless of the origin of the IC design. When this on-chip decoupling exists in parallel with off-chip decoupling of lesser impedance, all interference currents will be forced off-chip rather than remaining confined within the tiny silicon chip area. An increase in the current loop area increases the amount of direct RF emissions from the IC package. Also, forcing the decoupling current to flow off-chip will cause ground bounce between the PCB reference plane and the silicon substrate. Specifically, $V_n$-net will become superimposed on all signal input and output lines connected to the IC and will cause all PCB traces to radiate as well.

A simple model will demonstrate the effect of the on-chip circuitry on the ultimate utility of the IC packages and PCB application. Typically, whatever occurs off-chip has little effect on on-chip circuitry at frequencies above 300 MHz, or even less. Essentially, when designed as a transmission line, the speed of charge transfer from off-chip to on-chip should not exceed the propagation delay of the package design—or even worse, exceed the LC time-constant of on-chip capacitance working in conjunction with the package interconnect, lead frame, and bond wire.

**ON-CHIP SOURCE REPRESENTATION**

The on-chip interference source can be described as an AC or time-dependent current source in parallel to an on-chip capacitance (with some internal series resistance). In literature, this kind of noise source is often denoted by ICEM or LECC models representing the behavior of the core of a digital IC. For off-chip interfaces, the IBIS model is frequently used. In fact, version 4.1 and above are particularly well suited to the analysis of both signal and power integrity. For the purpose of EMC calculations, all AC or time-dependent currents through all the pins of the IC must be taken into account before a reasonable calculation of RF emissions can take place.

Achieving an effective AC or time-dependent current characterization requires factoring in every aspect of the entire application—including transistor level IC design, the 3D extracted parameters of
the IC package, as well as all off-chip measures taken with regard to supply decoupling or signal loading. Alternatively, a limited suitable model can be defined.

When a load capacitance is measured at an output, and when that output signal transition is fast, then the signal peak current will be as high as the voltage swing divided by the output driver impedance—i.e., \( R_{\text{on}} \) of the switching output since the load capacitance represents an instantaneous short-circuit impedance. When the same transition is applied to a transmission line as a load, the output signal transition is fast, then the output signal peak current will be limited to the same transition. Thus, the output driver impedance—

\[ \text{supply voltage} \times \text{rise time} \]

is limited to the off-chip decoupling capacitance (decoupling constraints). Clearly, the peak output current will be blocked by the equivalent series inductance represented by the IC package.

**SUPPLY BOUNCE**

Safeguarding effective function and ensuring robust design of digital ICs necessitate on-chip voltage bounce that is equal, or less than, 10 percent of the nominal supply voltage. In the instance of nanometer CMOS designs, supply bounce values of 5 percent or less are recommended. In all these CMOS designs, a 10, or even 20, times larger switching capacitance on-chip is needed to compensate for the simultaneous switching capacitance on-chip. Adhering to this design dictum, a total on-chip capacitance of 1 nF means that a maximum 100 pF of capacitances (gate–oxide + interconnect) should be allowed to switch simultaneously. This on-chip decoupling constraint applies only to the cycle-to-cycle operation of the digital CMOS design and does not hold true for an instantaneous change of its operating condition.

When the IC is supplied from an external supply voltage regulator module (VRM) or an external power management unit (PMU), the response rate of these regulators is typically around several \( \mu \text{s} \) for both the linear and switching regulator versions. For example, consider a digital CMOS IC running with a 1-GHz clock and going from an idle to an active state. In this instance, the long-term average supply current goes up from \( \mu \text{A} \) or mA to amps. Essentially, a thousand clock cycles have passed before the voltage regulator reacts appropriately. An off-chip decoupling or buffer capacitor is necessary to provide the amount of charge \( (Q = \Delta t \cdot C \cdot \Delta V) \) needed to keep the supply voltage within limits during the response time of the regulator.

For example, when 1 amp is required over 1 \( \mu \text{s} \), 1 \( \mu \text{C} \) of charge is required. When the nominal supply voltage is 1.8 V, the delta voltage allowed is 180 mV. The buffer capacitance value between the IC to be decoupled and the voltage regulator must be 6 \( \mu \text{F} \), or slightly more, perhaps 8 \( \mu \text{F} \). With a 5 percent supply voltage tolerance, the buffer capacitance must be twice this value.

In synchronous single-frequency digital CMOS designs, the peak current is typically three to 10 times higher than the average current. In this example, the supply currents reach a peak of three to ten amps. The supply current must diminish to zero before the next clock edge, and all activity ceases just before the next clock phase. Given these constraints, the peak current pulse width must be three to 10 times shorter than the period width. With a 1-GHz clock, the figure should be 100 to 330 ps.

**RESONANCES**

Resonances are often observed between off-chip decoupling capacitances. In the case of electrolytic or small and large value ceramic devices, resonances also occur between the on-chip and off-chip capacitances. Clearly, the interference current produced by the IC will be multiplied by the quality of the resonant loop and will be radiated by the larger loop area and ground bounce voltage. The on-chip/off-chip resonance frequency is determined by the smallest capacitance value in that loop, typically the on-chip capacitance. This on-chip capacitance (with the total loop inductance) will determine the resonance frequency.
OFF-CHIP IC DECOUPLING MEASURES

With a leaded QFP package, the lead length will be 4 mm, yielding an equivalent total inductance of 8 nH. That total along with an on-chip capacitance of 8 nF produces a resonance frequency of about 20 MHz. This particular supply system will not allow a supply recovery faster than 17 ns, the time for the fastest slew rate. When coupled (transmission) lines are used between the on-chip and off-chip decoupling position, the inductance will be decimated.

Still, 1.7 ns will be too long for a 1-GHz clock operation. The distance or lead length must be shortened or another decoupling technique should be employed—e.g., integrating decoupling capacitance in or on the package as is done with most PC processors. In all cases, resonances will occur between the various decoupling positions, and these resonances can be determined using simple analog circuit simulators such as SPICE.

When the activity within the IC does not coincide with a resonance of the supply decoupling circuitry, few problems will occur. Unfortunately, when it does coincide because of a (sub-) harmonic of the clock and/or data, interference may shoot sky high, and the functionality of the IC may be compromised. (Note: also the harmonic frequencies are of importance.) When such interference occurs within a particular data stream or data pattern, it can be difficult to arrive at accurate simulations or to detect the problem within actual applications.

OFF-CHIP DECOUPLING

The conventional wisdom for achieving a stable supply voltage is to place decoupling capacitors in close proximity and to connect them to a PCB power plane structure of finite length with a proportionately lowered characteristic transmission line impedance. Support for this approach can be found in many sectors of the industry.

With this conventional decoupling technique, the impedance characteristic on-chip will fluctuate significantly as a result of frequency, the X-Y positioning on the PCB, and the location of other decoupling capacitors (Figure 1). It should be noted that resonances off-chip have little effect on the internal voltage; but at some frequencies, the noise off-chip is greater than that on-chip.

Other techniques for assuring a stable power supply involve the use of an RF-lossy low-pass filter at each supply position to attain current confinement. In effect, each IC supply node is isolated from the rest of the PCB. The filtering is achieved using an RF-lossy ferrite bead (e.g., $R = 100 \Omega \times 100$ MHz) as well as the decoupling capacitors mentioned earlier.

**ROBUST DECOUPLING**

Rather than focusing on the remaining disturbance voltage and the decoupling capacitors found off-chip, it would be prudent to calculate the remaining disturbance voltage on-chip and the resulting ground bounce. The off-chip decoupling current should be kept low and should not include any quality of the resonance frequencies of the decoupling capacitors designed for this approach can be found in many sectors of the industry.

**CONCLUSIONS**

The IC decoupling schemes typically
provided in application notes from various IC suppliers are intended to assure the function of the IC in its application. They do not, however, assure electromagnetic compatibility.

- Leaded packages such as a QFP function as a low-pass filter, but they cause higher RF emissions at higher frequencies (<100 MHz). See Figure 2.
- BGAs with TLM topology produce a greater level of resonances at higher frequencies (>100 MHz).
- Creating an isolated power island on the PCB is vital if interference is to be prevented from propagating throughout the PCB.

The decoupling measures taken off-chip have little effect on the on-chip supply bounce, but they can result in a serious escalation of resonances with a typical quality factor of 10 when compared with actual, realistic decoupling component values. Off-chip decoupling, or buffering, is a necessity, particularly in instances in which the IC has time-variant power consumption and active voltage regulators are used. Off-chip current paths can be confined using a Kelvin contact approach (see Interference Technology 2007 Test & Design Guide).

BIBLIOGRAPHY
Hideki Osaka, Daisuke Tanaka, Osami Wada, Yoshitaka Toyota, and Ryuji Koga, “Linear Equivalent Circuit and Current Source for I/O (LECCS-I/O) Modeling of IC Power Current for EMI Simulation, and


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Designing off-chip decoupling so that interference is forced off-chip is just one challenge where today’s sophisticated EMC design software packages can help. Visit the new InterferenceTechnology.com, and check out the “New Products” Listings. And be sure to look for special editions of the eNews focused on EMC Software.